In the Claims

1. (Currently amended) A thin film transistor substrate comprising self-assembled monolayers between the substrate and a metal wiring, the self-assembled monolayers being formed by the compounds selected from a group consisting of 3-aminopropyltrimethoxysilane, 3-aminopropyltriethoxysilane, 2-aminoundecyltrimethoxysilane, aminophenyltrimethoxysilane, N-(2-aminoethylaminopropyl)trimethoxysilane, methyltrimethoxysilane, propyltriacetoxysilane, (3-mercaptopropyl)trimethoxysilane and (3-mercaptopropyl)trimethoxysilane.

2. (Canceled)

3. (Original) A thin film transistor substrate according to claim 1, wherein thickness of the self-assembled monolayers ranges from 2 to 3 nm.

4. (Original) A thin film transistor substrate according to claim 1, wherein the metal wiring is made of copper or alloy of copper and metals selected from a group consisting of Ag, Mg, B, Ca, Al, Li, Np, Pu, Ce, Eu, Pr, La, Nd, Sm and Zn.

5. (Original) A thin film transistor substrate according to claim 1, wherein the substrate is a glass substrate, an n+a-Si/a-Si/SiN three-layer substrate, or an Si, $SiO_2$ or other low-k ($k<3.5$) substrate.

6. (Original) A thin film transistor substrate comprising:

an insulation substrate;

a first signal line formed on the insulation substrate;

a first insulation film formed on the first signal line;

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a second signal line formed on the first insulation film and crossing the first signal line;

a thin film transistor electrically connected with the first signal line and the second signal line;

a second insulation film formed on the thin film transistor and having a first contact opening that expose an electrode of the thin film transistor; and

a pixel electrode formed on the second insulation film and connected to an electrode of the thin film transistor through the first contact opening, wherein at least one of the first signal line and the second signal line has a copper or copper alloy wiring structure consisting of a double layer of self-assembled monolayers and a Cu layer.

7. (Original) A thin film transistor substrate according to claim 6, wherein at least one of the first signal line and the second signal line has a copper or copper alloy wiring structure consisting of three layers of self-assembled monolayers, an Ag layer and a Cu layer.

8. (Original) A thin film transistor substrate comprising:

a gate wiring formed on an insulation substrate and comprising a gate line and a gate electrode connected to the gate line;

a gate insulation film covering the gate wiring;

a semiconductor pattern formed on the gate insulation film;

a data wiring comprising a source electrode and a drain electrode formed in the same layer on the gate insulation film or on the semiconductor pattern, which are

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separated from each other, and a data line connected to the source electrode and crossing the gate line to define a pixel area; a protection film having a first contact opening that exposes the drain electrode; and

a pixel electrode formed on the protection film and connected with the drain electrode through the first contact opening, wherein at least one of the gate wiring and the data wiring has a copper or copper alloy wiring structure consisting of a double layer of self-assembled monolayers and a Cu layer.

9. (Original) A thin film transistor substrate comprising:

an insulation substrate;

a gate wiring formed on the substrate and comprising a gate line, a gate electrode and an end part of the gate line;

a gate insulation film formed on the gate wiring and having a contact opening that exposes the end part of the gate line;

a semiconductor pattern formed on the gate insulation film;

a data wiring comprising a source electrode, a drain electrode, a data line and an end part of the data line that has a contact layer pattern on the gate insulation film or on the semiconductor pattern;

a protection film formed on the data wiring and having contact openings that expose the end part of the gate line, the end part of the data line and the drain electrode; and

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a transparent electrode layer pattern electrically connected with the exposed end part of the gate line, end part of the data line and drain electrode, wherein at least one of the gate wiring and the data wiring has a copper or copper alloy wiring structure consisting of a double layer of self-assembled monolayers and a Cu layer.

10. (Original) A thin film transistor substrate according to claim 8 or claim 9, which further comprise an ohmic contact layer formed between the semiconductor pattern and the data wiring, wherein the ohmic contact layer has a structure substantially identical to that of the data wiring.

11. (Currently amended) A thin film transistor substrate according to claim 8 or claim 9, wherein the semiconductor pattern ~~has a structure identical to~~ is substantially the same pattern as that of the data wiring except the data wiring crosses the gate wiring ~~for the channel part~~.

12. (Currently amended) A metal wiring method of a thin film transistor substrate comprising:

a step of coating a coating composition for self-assembled monolayers (SAMs) formation on a substrate and heat-treating it;

a step of depositing a metal wiring material on the substrate; and

a step of heat-treating the substrate, wherein the coating composition for self-assembled monolyaers formation comprises the compounds selected from a group consisting of 3-aminopropyltrimethoxysilane, 3-aminopropyltriethoxysilane, 2-aminoundecyltrimethoxysilane, aminophenyltrimethoxysilane, N-(2-aminoethylaminopropyl)trimethoxysilane, methyltrimethoxysilane,

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propyltriacetoxysilane, (3-mercaptopropyl)trimethoxysilane and (3-mercaptopropyl) trimethoxysilane.

13. (Original) A copper wiring method of a thin film transistor substrate according to claim 12, wherein the substrate is a glass substrate, an n+a-Si/a-Si/SiN three-layer substrate, or an Si, $SiO_2$ or other low-k ($k<3.5$) substrate.

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